REMARKS

Claims 1-21 are pending in the application. Claims 1-8 have been amended and claims 9-21 are newly added to the application. No new matter has been introduced by the amendment.

Rejection Under 35 U.S.C. § 112, ¶ 2

Claim 7 has been rejected for reciting unclear subject matter. This rejection is overcome in view of the amendment of claim 7 to recite that a metal plate is electrically connected to one of the crossing points of metal leads in the cohesive latticed metal region of the first substructure. Claim 7 further recites that the metal plate is also electrically connected to electrically conductive regions of the second substructure. The electrical connections are accomplished by means of one or more respective via connections.

Rejection Under 35 U.S.C. § 103(a)

Claims 1-8 have been rejected over Arita et al. in view of Kuroda et al. This rejection is overcome in view of the amendment of claim 1 together with the following remarks.

Claim 1 recites a semiconductor component in which a capacitor structure resides in an insulating layer on a semiconductor substrate. The capacitor structure includes a first substructure that includes crossing metal leads which extend in a first common plane parallel to the substrate's surface. The first substructure also includes electrically conductive regions arranged in openings in the first cohesive lattice metal region. Claim 1 further recites that the semiconductor component includes a first connecting line electrically connected to the first cohesive lattice metal region and a second connecting line connected to the electrically conductive regions. The Applicant respectfully asserts that their claimed semiconductor component is not suggested or disclosed by Arita et al. or Kuroda et al. taken alone or in combination.

As acknowledged in the instant Office Action at page 4, Arita et al. fail to suggest or disclose the claimed capacitance structure. The Applicant respectfully asserts that the addition of Kuroda et al. does not overcome the deficiencies of Arita et al.

Kuroda et al. disclose a coupling capacitor for use in a wiring board, as illustrated in Figs. 17 and 18 of their drawing. The capacitor is essentially a box-like structure that includes numerous side electrodes exposed on the outer surface of the capacitor. Rather than a capacitor having latticed metal regions that include crossing metal leads, Kuroda et al. discloses a capacitor constructed from a series of overlying metal electrode plates. The plates are all essentially of the same geometry, but are rotated 90° relative to each other (as shown in Figs. 3A and 3B, elements 10 and 11). Accordingly, the capacitor disclosed by Kuroda et al. does not suggest or disclose a capacitor structure that includes crossing metal leads. Further, the capacitor of Kuroda et al. does not suggest or disclose different regions of a first substructure in which separate connecting lines are electrically connected to the different regions.

The Applicant respectfully asserts that there is no basis for the hypothetical interpretation of the structure disclosed by Kuroda et al. that appears at page 3 of the instant Office Action. Rather than disclosing any type of lattice structure, Kuroda et al. disclosed a series of overlying metal plates. Further, as described by Kuroda et al. at column 6, lines 6-18, the internal electrodes have shapes that are substantially identical to each other but are arranged so as to be rotated by about 90° relative to each other. The Applicant respectfully asserts that there is no suggestion within Kuroda et al. for a lattice structure or for the cross-hatched representation of Figure 8 that appears at page 3 of the instant Office Action.

Claims 2-8 are allowable in view of their direct or indirect dependence from Claim 1. These dependent claims further distinguish the Applicant's claimed semiconductor component from the cited references.

Claim 2, as amended, recites a second substructure including crossing metal leads in electrically conductive regions. The crossing metal leads and the electrically conductive regions of the second substructure are electrically connected to the first substructure by the first and second connecting lines.

because of the geometric relationship of the electrically conductive regions in the Applicant's capacitance structure. Further, the magnitude of the first non-parasitic capacitance differs from the magnitude of the second non-parasitic capacitance.

Claim 11 recites a semiconductor component having an integrated capacitance structure. The component includes a semiconductor substrate and an insulating layer overlying the surface of the semiconductor substrate. A capacitance structure resides in the insulating layer and includes first and second metal lattices, each having intersecting metal leads. The first and second lattices reside in first and second common planes that are parallel to the substrate surface. Electrically conductive regions are arranged in openings in the first and second metal lattices. The electrically conductive regions are spaced apart from edge regions of the openings by the insulating layer. The first and second metal lattices are laterally offset from one another, such that the electrically conductive regions on the first metal lattice are substantially vertically above crossing points of the second metal lattice, and vice versa. First and second electrical connections are included between the first and second lattices, such that these electrical connections have different electric potentials.

Claims 12-15 recite additional features of the semiconductor component of Claim 11. Claim 12 recites that the electrically conductive regions comprise metal plates or node points.

Claim 13 recites that the electrical connections comprise first and second connecting lines that connect the electrically conductive regions and the crossing points of the first and second metal lattices.

Claim 14 recites that the semiconductor component further comprise a metal plate in a third common plane parallel with substrate surface. The metal plate is electrically coupled to the first and second metal lattices by the first and second electrical connections.

Claim 15 recites that the semiconductor component further comprise a third metal lattice that includes intersecting metal leads in a third plane parallel to the substrate surface. The intersecting metal leads define openings that are devoid of

electrically conductive regions. The intersecting metal leads are electrically connected to the first and second metal lattices by the electrical connections.

Claim 16 recites a semiconductor component having an integrated capacitance structure. The capacitance structure includes an insulating layer and first and second metal lattices in the insulating layer. The first and second metal lattices include intersecting metal leads and positioned in respective common planes. Electrically conductive regions are arranged in openings in at least one of the first and second metal lattices. The electrically conductive regions are spaced apart from edge regions of the openings by the insulating layer. The first and second metal lattices are laterally offset from one another, such that the electrically conductive regions or the first metal lattice are substantially vertically above crossing points of the second metal lattice, and vice versa. A third metal structure resides in the insulating layer in a third common plane. The third metal structure comprises either a third metal lattice or a metal plate. First and second electrical connections reside between the first and second lattices and the third metal structure. The first and second electrical connections are at different electrical potentials.

Claims 17-21 depend either directly or indirectly from Claim 16. These claims are allowable in view of their dependence from Claim 16.

Claim 17 recites that the third metal structure comprises a metal plate coupled to the electrically conductive regions of the first and second metal lattices by the first and second electrical connections.

Claim 18 recites that the third metal structure comprise a third metal lattice. The intersecting metal leads are electrically connected to the electrically conductive regions of the first and second metal lattices by the first and second electrical connections.

Claim 19 recites that the first and second electrical connections electrically connect the electrically conductive regions of the first metal lattice to the crossing points of the second metal lattice and vice versa.

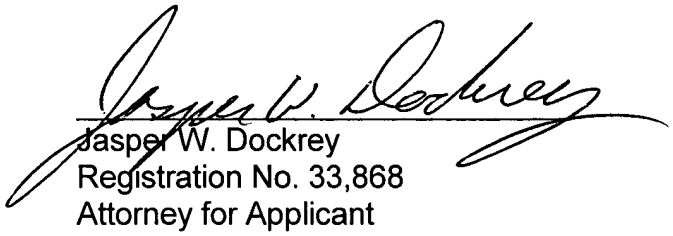
Claim 20 recites that the third metal structure comprise a third metal lattice including intersecting metal leads in electrically conductive regions and openings defined by the intersecting metal leads.

The Applicant respectfully asserts that the semiconductor component recited in Claims 9-21 are not suggested or disclosed by the combination of cited references, taken alone or in combination.

Claim 21 recites that non-parasitic capacitances exist between the electrically conductive regions and the intersecting metal leads of the first, second, and third metal lattices. The non-parasitic capacitances exist between the first and second connecting lines.

The Applicant has made a novel and non-obvious contribution to the art of semiconductor component design. The claims at issue distinguish over the cited references and are in condition for allowance. Accordingly, such allowances now are earnestly requested.

Respectfully submitted,



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